In the Claims:

1. (Currently Amended) A semiconductor, comprising:

a semiconductor wafer having a plurality of integrated circuit chips thereon, ~~such~~ said chips being separated by separating regions in the wafer, ~~such~~ said wafer having a plurality of electrical contacts;

a ~~self-supporting~~ planar dielectric member having an inner surface and an outer surface and defining an electrical conductor on said inner surface, said planar dielectric member positioned above said semiconductor wafer with said inner surface toward said circuit chips, and said ~~thereon, such electrical conductor being elevated above the regions in the fractional portion of the wafer, such~~ electrical conductor being electrically connected to the plurality of electrical contacts to electrically interconnect such plurality of chips, ~~portions of the dielectric member with~~ and to space said planar dielectric member from said semiconductor wafer, portions of the electrical conductor on said dielectric member ~~thereon~~ spanning ~~the~~ said separating regions in the wafer, and

a plurality of voltage generators, each one being associated with, and disposed adjacent to, a corresponding one of the chips.

2-5 (Cancelled)

6. (Currently Amended) A semiconductor, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the fractional portion of the wafer;

a plurality of sets of electrical components, each set being associated with, and adjacent to, a corresponding one of the chips; and

a ~~self-supporting~~ planar dielectric member having an inner surface and an outer surface and defining an electrical conductor ~~thereon~~ on said inner surface, said planar dielectric member positioned above said semiconductor wafer with said inner surface toward said circuit chips and a portion of said electrical conductor electrically connecting the plurality of ~~electrical~~ selected one or ones of the electrical components to the chips and spacing said planar dielectric member, from said ~~with portions of the electrical conductor elevated above the regions in the~~ fractional portion of the wafer ~~and~~, portions of the electrical conductor on said planar dielectric member spanning the separating regions between the chips in the fractional portion of the wafer.

7. (Previously Presented) The semiconductor recited in claim 6 wherein each set of electrical components includes a plurality of different electrical components.

8. (Withdrawn) A method for forming a semiconductor, comprising:

providing a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the fractional portion of the wafer,

providing a plurality of sets of electrical components, each set being associated with, and adjacent to, a corresponding one of the chips; and

providing an electrical conductor to electrically connect a selected one or ones of the electrical components to the chips with portions of the electrical conductor spanning the separating regions between the chips in the fractional portion of the wafer.

9. (Withdrawn) The method recited in claim 8 wherein each set is provided with a plurality of different electrical components.

10. (Withdrawn) The semiconductor recited in claim 6 including

a fusible link electrically connecting a bus disposed in at least one of the plurality of integrated circuit chips and a corresponding one of the plurality of electrical components.

11. (Previously Presented) A semiconductor, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the fractional portion of the wafer;

a plurality of sets of electrical components, each set being associated with, and adjacent to, a corresponding one of the chips; and

an electrical conductor electrically connecting the plurality of electrical selected on or ones of the electrical components to the chips with portions of the electrical conductor elevated above the regions in the fractional portion of the wafer and spanning the separating regions between the chips in the fractional portion of the wafer; and

wherein each one of the electrical components is disposed in the separating region.

12. (Previously Presented) The semiconductor recited in claim 11 wherein the electrical components are voltage generators.

13. (Previously Presented) The semiconductor recited in claim 12 wherein the voltage generators are interconnected by the conductor elevated above the regions in the fractional portion of the wafer.

14. (Withdrawn) The semiconductor recited in claim 10 wherein the fusible link is disposed in disposed in at least one of the plurality of integrated circuit chips.

15. (Previously Presented) The semiconductor recited in claim 12 wherein at least one of the voltage generators is coupled to more than one bus in corresponding ones of the plurality of integrated circuit chips.

16. (Currently Amended) A semiconductor package, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer, such fractional portion of the wafer having a plurality of electrical contacts;

a ~~self-supporting~~ planar dielectric member having an inner surface and an outer surface and defining an electrical conductor ~~thereon, such~~ on said inner surface, said planar dielectric member positioned above said fractional portion of said semiconductor wafer with said inner surface toward said circuit chips, said electrical conductor being electrically connected to the plurality of electrical contacts to electrically interconnect such plurality of chips and to space said planar dielectric member from said fractional portion of said semiconductor wafer, portions of the electrical conductor on said planar dielectric member spanning the regions in the fractional portion of the wafer; and

a plurality of voltage generators, each one being associated with, and disposed adjacent to, a corresponding one of the chips.

17. (Previously Presented) A semiconductor package, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer, such fractional portion of the wafer having a plurality of electrical contacts;

a dielectric member having an electrical conductor hereon, such electrical conductor being electrically connected to the plurality of electrical contacts to electrically interconnect such plurality of chips, portions of the electrical conductor spanning the regions in the fractional portion of the wafer; and

a plurality of voltage generators, each one being associated with, and disposed adjacent to, a corresponding one of the chips; and

wherein each one of the voltage generators in disposed in the separating region.

18. (Currently Amended) A semiconductor package, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer, such fractional portion of the wafer having a plurality of electrical contacts;

a ~~self-supporting~~ planar dielectric member having an inner surface and an outer surface and defining an electrical conductor ~~thereon~~ on said inner surface, said planar dielectric member positioned above said fractional portion of said semiconductor wafer with said inner surface toward said circuit chips, and said electrical conductor electrically connected to the plurality of

electrical contacts of the plurality of chips to electrically interconnect such plurality of chips and to space said planar dielectric member from said fractional portion of said semiconductor wafer, portions of the electrical conductor spanning the regions in the fractional portion of the wafer, ~~such conductor being elevated above the regions in the fractional portion of the wafer~~; and

a plurality of voltage generators, each one being associated with, and disposed adjacent to, a corresponding one of the chips.

19. (Cancelled)

20. (Currently Amended) A semiconductor package arrangement, comprising:

(A) a printed circuit board having an electrical interconnect thereon;

(B) a semiconductor package, comprising:

(i) a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer, such fractional portion of the wafer having a plurality of electrical contacts;

(ii) a ~~self-supporting~~ planar dielectric member having an inner surface and an outer surface and defining an electrical conductor ~~thereon~~ on said inner surface, said planar dielectric member positioned above said fractional portion of said semiconductor wafer with said inner surface toward said circuit chips, and said electrical conductor electrically connected to the plurality of electrical contacts of the plurality of chips to electrically interconnect such plurality of chips, and to space said planar dielectric member from said fractional portion of said semiconductor wafer, portions of the electrical conductor spanning the regions in the fractional portion of the wafer; and

(iii) a plurality of voltage generators, each one being associated with, and disposed adjacent to, a corresponding one of the chips; and

(C) a via conductor extending from said inner surface to said outer surface of said dielectric member for electrically connecting the electrical conductor of the package to the electrical interconnect of the printed circuit board.

21. (Previously Presented) A semiconductor package arrangement, comprising:

(A) a printed circuit board having an electrical interconnect thereon;

(B) a semiconductor package, comprising:

(i) a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer, such fractional portion of the wafer having a plurality of electrical contacts;

(ii) an electrical conductor electrically connected to the plurality of electrical contacts of the plurality of chips to electrically interconnect such plurality of chips, portions of the electrical conductor spanning the regions in the fractional portion of the wafer; and

(iii) a plurality of voltage generators, each one being associated with, and disposed adjacent to, a corresponding one of the chips; and

(C) a conductor for electrically connecting the electrical conductor of the package to the electrical interconnect of the printed circuit board; and

wherein each one of the voltage generators is disposed in the separating region.

22. (Currently Amended) The semiconductor recited in claim 1 wherein the ~~self-supporting~~ planar dielectric member is a printed circuit board.

23. (Currently Amended) The semiconductor recited in claim 6 wherein the ~~self-supporting~~ planar dielectric member is a printed circuit board.

24. (Currently Amended) The semiconductor recited in claim 16 wherein the ~~self-supporting~~ planar dielectric member is a printed circuit board.

25. (Currently Amended) The semiconductor recited in claim 18 wherein the ~~self-supporting~~ planar dielectric member is a printed circuit board.

26. (Currently Amended) The semiconductor recited in claim 20 wherein the ~~self-supporting~~ planar dielectric member is a printed circuit board.

27. (New) A semiconductor, comprising:

a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the wafer, such wafer having a plurality of electrical contacts;

a dielectric member having an electrical conductor thereon, such electrical conductor being elevated above the regions in the fractional portion of the wafer, such electrical conductor being electrically connected to the plurality of electrical contacts to electrically interconnect such plurality of chips, portions of the dielectric member with portions of the electrical conductor thereon spanning the regions in the wafer, and

a plurality of voltage generators disposed in the separating regions, each one being associated with, and disposed adjacent to, a corresponding one of the chips.

28. (New) A semiconductor package, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer, such fractional portion of the wafer having a plurality of electrical contacts;

a dielectric member having an electrical conductor thereon electrically connected to the plurality of electrical contacts of the plurality of chips to electrically interconnect such plurality of chips, portions of the electrical conductor spanning the regions in the fractional portion of the wafer, such conductor being elevated above the regions in the fractional portion of the wafer; and

a plurality of voltage generators disposed in the separating region, each one being associated with, and disposed adjacent to, a corresponding one of the chips.